ZCU102 I2C

Tuesday, January 2, 2024

2:48 PM

The ZCU102 board uses the PS I2C\_0 and I2C\_1 ports for additional GPIO and for driving multiple I2C buses.

I2C\_0 connects to two port-expander devices (for GPIO) and one 4:1 I2C bus switch.

I2C\_1 connects to two 8:1 I2C bus switches. The U135 device provides access to the I2C devices on the Abaco FMC216 DAC boards mounted on the two ZCU high density FMC (HPC) connectors.

The Abaco boards each have an I2C EEPROM, an AD7291 voltage monitor, and a CPLD.

The CPLD registers provide a method to talk to the LMK04828 clock chip and the four DAC39J84 4-channel DACs over a 32-bit SPI bus.

To write a register on one of the FMC216 DAC devices the PS must first write to the I2C\_1 switch (U135) at address 0x75 to enable one, or both, of the FMC I2C buses. The switch only has one register with a single bit to enable each output bus.

Then the CPU can write to the CPLD on the Abaco boards. To write a 32-bit value to the clock or to the DACs the CPU loads 8-bit data into four registers (reg-6, -7 ,-8, -9) in the CPLD and then selects the target device(s) by setting '1' in bits of CPLD reg-0.

CPLD reg-1 and reg-2 bits control DAC enable sleep, reset, and output amplifier signals.

**ZCU102 I2C0 (MIO 14-15)**

I2C0 connects to MPSoC U1 PS Bank 500 and PL bank 50, and to system controller U41, as

shown in Figure 3-17. I2C0 connects to two GPIO 16-bit port expanders (TCA6416A U61 and

U97) and an I2C SWITCH (PCA9544A U60) for controlling resets, GTR multiplexer settings,

and the power system enable pins, without requiring the PL-side to be configured. TCA6416A

U97 is pin-strapped to respond to I2C address 0x20, and U61 to 0x21. The PCA9544A

multiplexer is set to 0x75.

The I2C0 bus also provides access to the PMBUS power controllers and PS-side and PL-side

INA226 power monitors via the U60 PCA9544A bus switch. All PMBus controlled Maxim

regulators are tied to the MAXIM\_PMBUS, while the INA226 power monitors are separated

on to PS\_PMBUS and PL\_PMBUS. Figure 3-17 shows the I2C0 bus topology.

Table 3-19 lists the I2C0 port expander TCA6416A U61 connections and Table 3-20 the

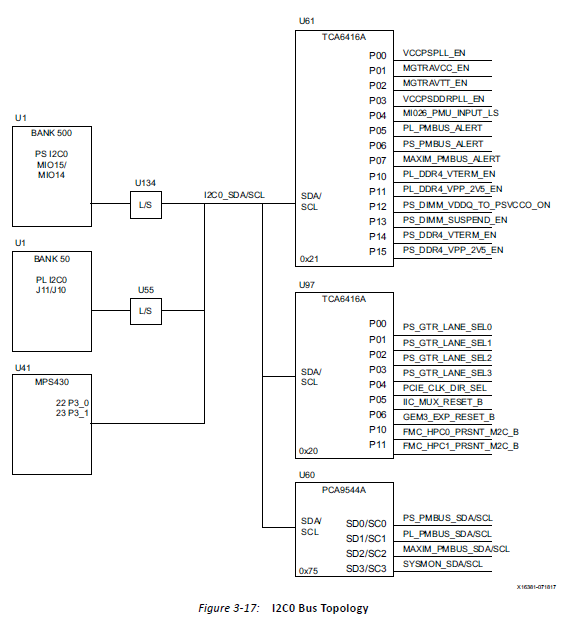
TCA6416A U97 connections. The devices on each bus of the I2C0 multiplexer U60 are

identified in Table 3-21 and the multiplexer bus connections are listed in Table 3-22.

The important GPIO signals on I2C\_0 are :

Pin P05 on U97 which drives the reset for the I2C\_1 switches U34 and U135.

Pins P10 and P11 on U97 which are the board present indicators for the FMC\_HPC0/1 connectors.



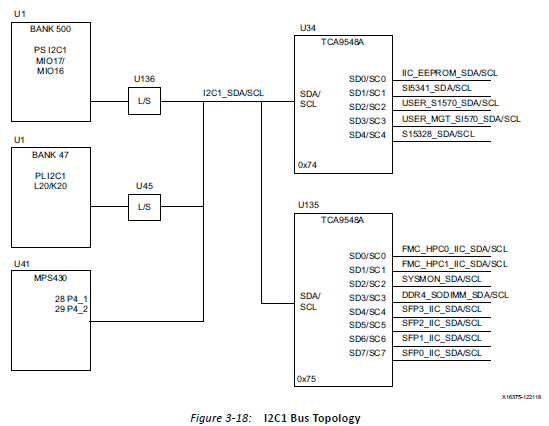
**ZCU102 I2C1 (MIO 16-17)**

The PS-side I2C1 interface provides access to I2C peripherals through a set of I2C switches.

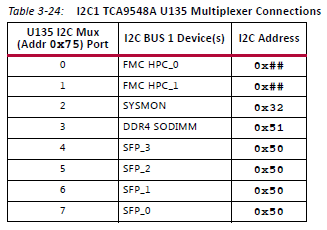
The I2C connection is shared with the PL-side and the system controller. Figure 3-18 shows

a high-level view of the I2C1 bus connectivity represented in Table 3-23 and Table 3-24.

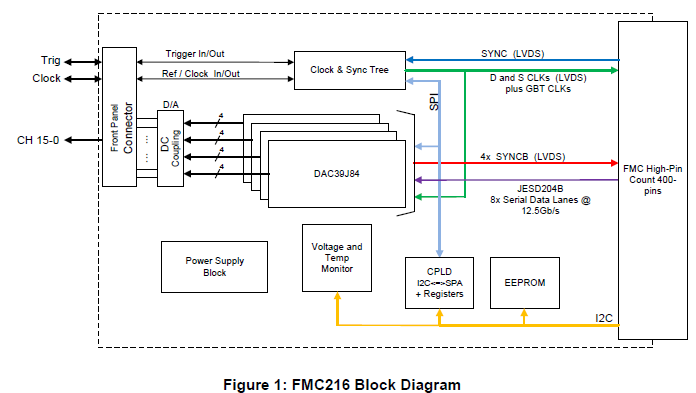
TCA9548A U34 is set to 0x74 and TCA9548A U135 is set to 0x75.



U125 outputs FMC\_HPC\_0 and FMC\_HPC\_1 are connections to the Abaco DAC boards.



**Abaco DAC Board I2C/SPI diagram**



**Software tasks for I2C testing of board control.**

1. Read ZCU102 I2C\_0 port-expander device U67 at address 0x20 and print the status of P05 (I2C\_MUX\_RESET\_B) and P10, P11 (the FMC board detect inputs). The port expander devices have input level, output level, direction and inversion registers. All ports are inputs by default.
2. Write to ZCU102 I2C\_1 mux device U135 at address 0x75, to set bit-0 in the control register to steer I2C\_1 bus activity to the Abaco board on FMC\_0 (or set bit-1 for I2C\_1 access to FMC\_1).
3. Read Abaco CPLD Firmware version from register-5 to test the I2C connection to the Abaco board.
4. (Optional) Read temperature from the FMC216 AD7291 register-02. temp = value/4
5. Use the CPLD to read the ID\_DEVICE\_TYPE field from register 0x003 on the LMK04828 device over the SPI bus.
6. Read a register from each of the four DAC chips. Reset all FMC DACs?

Multiple I2C devices on FMC HPC\_0 and FMC HPC\_1